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The latest advances in three-dimensional integrated circuit stacking technology With a focus on industrial applications, 3D IC Stacking Technology offers comprehensive coverage of design, test, and fabrication processing methods for three-dimensional device integration.

Wafer-level bonding/stacking technology for 3D integration ...

1. Introduction Three-dimensional integrated circuits (3D IC) has been generally acknowledged as the next generation semiconductor technology with the advantages of small form factor, high-performance, low power consumption, and high density integration . . . Through silicon via (TSV) and stacked bonding are the core

technologies to perform

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### **What is 3D Integration? - 3D InCites**

3D ICs can be divided into 3D Stacked ICs (3D-SICs), which refers to stacking IC chips and interconnecting them with TSVs; and true 3D ICs, which use fab processes to stack multiple device layers on a single chip, which may or may not use very-fine-pitch TSVs to form the interconnect.

### **Three-dimensional integrated circuit - Wikipedia**

In microelectronics, a three-dimensional integrated circuit (3D IC) is an integrated circuit manufactured by stacking silicon wafers or dies and interconnecting them vertically using, for instance, through-silicon vias (TSVs) or Cu-Cu connections, so that they behave as a single device to achieve performance improvements at reduced power and

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### **The future of computers: 3D chip stacking - ExtremeTech**

In a few weeks, Intel will release Ivy Bridge, the first mass-produced 22nm parts, and more importantly the first to use 3D tri-gate FinFET transistors.

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ECTC PDC , 2009 3 Lau Lau, TSV (Through-Silicon Via)  
William Shockley (1956 Nobel laureate, co-invented the transistor) filed a patent Semiconductive Wafer and (g transistor) filed a patent, Semiconductive Wafer and Method of Making the Same on October 23, 1958 and was granted

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